AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions of the claims and all prior listings of the claims in the present application.

1. (currently amended) A channel state measurement apparatus for a receiver, comprising:

a direct channel state measurement unit ~~for receiving~~ adapted to receive complex symbol streams, [[for]] adapted to perform[[ing]] de-mapping on the complex symbol streams, ~~for calculating~~ adapted to calculate an error signal based on the received complex symbol streams and de-mapped complex symbol streams, and ~~for generating~~ adapted to generate direct channel state information based on the calculated error signal;

an indirect channel state measurement unit ~~for generating~~ adapted to generate indirect channel state information based on a magnitude of a channel frequency response;

a co-channel interference detection unit ~~for generating~~ adapted to generate a channel state selection control signal based on the calculated error signal and the magnitude of the channel frequency response; and

a selection unit [[for]] adapted to selectively output[[ting]] one of the direct channel state information and the indirect channel state information[[,]] based on a logic state of the channel state selection control signal.

2. (currently amended) The apparatus of claim 1, wherein the direct channel state measurement unit comprises:

a first de-mapping and pilot insertion unit [[for]] adapted to insert[[ing]] a given pilot into an I stream of the complex symbol streams, [[for]] adapted to perform[[ing]] de-mapping on the I stream, and [[for]] adapted to output[[ting]] the de-mapped I stream;

a first subtraction unit [[for]] adapted to subtract[[ing]] the de-mapped I stream from the I stream to output a first subtraction result;

a first squaring unit ~~for squaring~~ adapted to square the first subtraction result to output a first squaring result;

a second de-mapping and pilot insertion unit [[for]] adapted to insert[[ing]] the given pilot into a Q stream of the complex symbol streams, [[for]] adapted to perform[[ing]] de-mapping on the Q stream, and [[for]] adapted to output[[ting]] the de-mapped Q stream;

a second subtraction unit [[for]] adapted to subtract[[ing]] the de-mapped Q stream from the Q stream to output a second subtraction result;

a second squaring unit ~~for squaring~~ adapted to square the second subtraction result to output a second squaring result;

a summation unit [[for]] adapted to sum[[ming]] the first squaring result and the second squaring result to output a summed value;

an averaging unit ~~for averaging~~ adapted to average a summed value output from the summation unit during a current symbol duration and a summed value output from the summation unit during a previous symbol duration to output the calculated error signal; and

a non-uniform quantizing unit ~~for quantizing~~ adapted to quantize the calculated error signal by inverting the calculated error signal using a non-uniform transfer function to output the direct channel state information.

3. (original) The apparatus of claim 1, wherein the indirect channel state information is a signal obtained by quantizing the magnitude of the channel frequency response with a uniform transfer function.

4. (currently amended) The apparatus of claim 1, wherein the co-channel interference detection unit comprises:

a third squaring unit ~~for squaring~~ adapted to square the magnitude of the channel frequency response to output a third squaring result;

a multiplication unit [[for]] adapted to multiply[[ing]] the third squaring result[[s]] and the error signal to output a multiplication result signal;

a frequency impulse response (FIR) filter ~~for integrating~~ adapted to integrate given carriers included in the multiplication result signal based on non-recursive filtering to provide an integrated signal;

a third subtraction unit [[for]] adapted to subtract[[ing]] first coefficient information from the integrated signal to output a third subtraction result;

a negative value discarding unit [[for]] adapted to discard[[ing]] a negative-valued third subtraction result and adapted to output[[ing]] a positive-valued third subtraction result as an output signal;

an accumulating unit ~~for accumulating~~ adapted to accumulate the output signal during one symbol duration to output an accumulation result;

a symbol averaging filter ~~for averaging an~~ adapted to average the accumulation result output from the accumulating unit during a current symbol duration with [[an]] the accumulation result output during a previous symbol duration to output an averaged signal;

a first comparator ~~for comparing~~ adapted to compare the averaged signal with second coefficient information to output first comparison information;

a second comparator ~~for comparing~~ adapted to compare the averaged signal with third coefficient information to output second comparison information; and

a logic circuit [[for]] adapted to output[[ting]] the channel state selection control signal based on a logic state of one of the first comparison information and the second comparison information.

5. (currently amended) The apparatus of claim 4, wherein the logic circuit outputs the channel state selection control signal:

at a second logic state, if the first comparison information is at the second logic state, or

at a first logic state, if the second comparison information is at the second logic state, or

at its previous logic state, if one of the first comparison information and the second comparison information is at the first logic state.

6. (currently amended) The apparatus of claim 1, wherein the co-channel interference detection unit comprises:

a third squaring unit ~~for squaring~~ adapted to square the magnitude of the channel frequency response to output a third squaring result;

a first multiplication unit [[for]] adapted to multiply[[ing]] the third squaring [[unit]] result and the error signal to output a first multiplication result;

a first switching circuit ~~for enabling~~ adapted to enable output of the first multiplication result based on a logic state of interference-affected carrier information;

a first accumulating unit ~~for accumulating~~ adapted to accumulate the first multiplication result, if received from the first switching unit, during one symbol duration to output a first accumulation result;

a second switching circuit ~~for enabling~~ adapted to enable output of the first multiplication result based on a logic state of non-interference-affected carrier information;

a second accumulating unit ~~for accumulating~~ adapted to accumulate the first multiplication result, if received from the second switching unit, during one symbol duration to output a second accumulation result;

a second multiplication unit [[for]] adapted to multiply[[ing]] the second accumulation result and [[a]] first coefficient information ~~together~~ to output a second multiplication result;

a third subtraction unit [[for]] adapted to subtract[[ing]] the second multiplication result from the first accumulated result to output a third subtraction result;

a symbol averaging filter ~~for averaging~~ adapted to average a[[n]] third subtraction result output from the third subtraction unit during a current symbol duration with a third subtraction result output during a previous symbol duration to output an averaged signal;

a first comparator ~~for comparing~~ adapted to compare the averaged signal with second coefficient information to output first comparison information;

a second comparator ~~for comparing~~ adapted to compare the averaged signal with third coefficient information to output second comparison information; and

a logic circuit [[for]] adapted to output[[ting]] the channel state selection control signal based on a logic state of one of the first comparison information and the second comparison information.

7. (currently amended) The apparatus of claim 6, wherein the logic circuit outputs the channel state selection control signal:

at a second logic state, if the first comparison information is at the second logic state, or

at a first logic state, if the second comparison information is at the second logic state, or

at its previous logic state, if one of the first comparison information and the second comparison information is at the first logic state.

8. (currently amended) The apparatus of claim 6, wherein the first switching [[unit]] circuit only outputs the first multiplication result to the first accumulating unit if the logic state of the interference-affected carrier information is in a second logic state[[;]], and

wherein the second switching [[unit]] circuit only outputs the first multiplication result to the second accumulating unit if the logic state of the non-interference-affected carrier information is in [[a]] the second logic state.

9. (currently amended) The apparatus of claim 1, wherein the receiver is a digital video broadcasting-terrestrial (DVB-T) receiver.

10. (currently amended) A method of providing channel state information in a receiver, comprising:

(a) generating direct channel state information based on a calculated error signal;

(b) generating indirect channel state information based on a magnitude of a channel frequency response;

(c) generating a channel state selection control signal based on the calculated error signal and the magnitude of the channel frequency response; and

(d) selectively outputting one of the direct channel state information and the indirect channel state information based on a logic state of the channel state selection control signal.

11. (currently amended) The method of claim 10, wherein step (a) comprises:

(a1) inserting a given pilot into an I stream of a plurality of received complex symbol streams;

(a2) de-mapping the I stream to output a de-mapped I stream;

(a3) subtracting the de-mapped I stream from the I stream to output a first subtraction result;

(a 4) squaring the first subtraction result to output a first squaring result;

(a5) inserting the given pilot into a Q stream of the received complex symbol streams;

(a6) de-mapping the Q stream to output a de-mapped Q stream;

(a7) subtracting the de-mapped Q stream from the Q stream to output a second subtraction result;

(a8) squaring the second subtraction result to output a second squaring result;

(a9) summing the first squaring result and the second squaring result to output a sum;

(a10) averaging the sum output during a current symbol duration and the sum output during a previous symbol duration to generate a calculated error signal; and

(a11) quantizing the calculated error signal by inverting the calculated error signal using a non-uniform transfer function to generate the direct channel state information.

12. (original) The method of claim 10, wherein the indirect channel state information is a signal obtained by quantizing the magnitude of the channel frequency response with a uniform transfer function.

13. (currently amended) The method of claim 10, wherein step (c) comprises:

(c1) squaring the magnitude of the channel frequency response to output a third squaring result;

(c2) multipl ying the third squaring result and the calculated error signal ~~together~~ to output a multiplication result;

(c3) integrating given carriers included in the multiplication result using non-recursive filtering to output an integration result;

(c4) subtracting first coefficient information from the integration result to output a third subtraction result;

(c5) discarding a negative-valued third subtraction result, else outputting a positive-valued third subtraction result as an output signal;

(c6) accumulating the output signal during one symbol duration to generate an accumulation result;

(c7) averaging the accumulation result for a current symbol duration and [[an]] the accumulation result during a previous symbol duration to output an averaged signal;

(c8) comparing the averaged signal with second coefficient information[[,]] to generate first comparison information;

(c9) comparing the averaged signal with third coefficient information to generate second comparison information; and

(c10) generating the channel state selection control signal based on a logic state of one of the first comparison information and the second comparison information.

14. (currently amended) The method of claim 13, wherein step (c10) includes:

(c101) generating the channel state selection control signal at a second logic state, if the first comparison information is at the second logic state, or

(c102) generating the channel state selection control signal at a first logic state, if the second comparison information is at the second logic state, or

(c103) generating the channel state selection control signal at its previous logic state, if one of the first comparison information and the second comparison information is at the first logic state.

15. (currently amended) The method of claim 10, wherein step (c) comprises:

(c1) squaring the magnitude of the channel frequency response to output a third squaring result;

(c2) multipl ying the third squaring result [[with]] and the calculated error signal to output a first multiplication result;

(c3) outputting the first multiplication result, if [[an]] interference-affected carrier information is in a given logic state;

(c4) accumulating the first multiplication result corresponding to the interference-affected carrier information during one symbol duration to output a first accumulation result;

(c5) outputting the first multiplication result, if [[a]] non-interference-affected carrier information is in [[a]] the given logic state;

(c6) accumulating the first multiplication result corresponding to the non-interference-affected carrier information during one symbol duration to output a second accumulation result;

(c7) multiplying the second accumulation result and first coefficient information to output a second multiplication result;

(c8) subtracting the second multiplication result from the first accumulation result to output a third subtraction result;

(c9) averaging the third subtraction result for a current symbol duration and the third subtraction result for a previous symbol duration to output an averaged signal;

(c10) comparing the averaged signal with second coefficient information[[,]] to generate first comparison information;

(c11) comparing the averaged signal with third coefficient information to generate second comparison information; and

(c12) generating the channel state selection control signal based on a logic state of one of the first comparison information and the second comparison information.

16. (currently amended) The method of claim 15, wherein step (c12) includes:

(c121) generating the channel state selection control signal at a second logic state, if the first comparison information is at the second logic state, or

(c122) generating the channel state selection control signal at a first logic state, if the second comparison information is at the second logic state, or

(c123) generating the channel state selection control signal at its previous logic state, if one of the first comparison information and the second comparison information is at the first logic state.

17. (currently amended) In a channel state measurement apparatus of a receiver, a co-channel interference detector ~~for providing~~ adapted to provide a selection control signal to selectively output one of direct channel state information determined from a calculated error signal and indirect channel state information determined from a channel frequency response, comprising:

a multiplier [[for]] adapted to multiply[[ing]] a squared value of [[the]] a magnitude of the channel frequency response and the calculated error signal to output a multiplication result;

a filter ~~for integrating~~ adapted to integrate the multiplication result to output an integration result;

a subtractor [[for]] adapted to subtract[[ing]] given coefficient information from the integration result to output a subtraction result;

a discarding unit [[for]] adapted to discard[[ing]] a negative-valued subtraction result[[,]] and [[else]] adapted to output[[ting]] a positive-valued subtraction result as an output signal;

an accumulator ~~for accumulating~~ adapted to accumulate the output signal during one symbol duration to generate an accumulation result;

an averager ~~for averaging~~ adapted to average the accumulation result for a current duration and an accumulation result during a previous duration to output an averaged signal to be used for generating first and second comparison information; and

a logic unit ~~for generating~~ adapted to generate the selection control signal based on a logic state of one of the first comparison information and the second comparison information.

18. (currently amended) The detector of claim 17, wherein the logic unit generates the selection control signal:

at a high logic state, if the first comparison information is at the high logic state, or

at a low logic state, if the second comparison information is at the high logic state, or

at its previous logic state, if one of the first comparison information and the second comparison information is at the low logic state.

19. (currently amended) In a channel state measurement apparatus of a receiver, a co-channel interference detector ~~for providing~~ adapted to provide a selection control signal to selectively output one of direct channel state information determined from a calculated error signal and indirect channel state information determined from a channel frequency response, comprising:

a first multiplier [[for]] adapted to multiply[[ing]] a square value of [[the]] a magnitude of the channel frequency response with the calculated error signal to output a first multiplication result;

a first switching circuit [[for]] adapted to output[[ting]] the first multiplication result[[,]] if [[an]] interference-affected carrier information is in a given logic state;

a first accumulator ~~for accumulating~~ adapted to accumulate the first multiplication result during a given duration to output a first accumulation result;

a second switching circuit [[for]] adapted to output[[ting]] the first multiplication result[[,]] if [[a]] non-interference-affected carrier information is in [[a]] the given logic state;

a second accumulator ~~for accumulating~~ adapted to accumulate the first multiplication result during a given duration to output a second accumulation result;

a second multiplier adapted to multiply the second accumulation result and a [[given]] coefficient to output a second multiplication result;

a subtractor [[for]] adapted to subtract[[ing]] the second multiplication result from the first accumulation result to output a subtraction result;

an averager ~~for averaging~~ adapted to average the subtraction result for a current duration and a subtraction result during a previous duration to output an averaged signal to be used for generating first and second comparison information; and

a logic unit ~~for generating~~ adapted to generate the selection control signal based on a logic state of one of the first comparison information and the second comparison information.

20. (currently amended) The detector of claim 19, wherein the logic unit generates the selection control signal:

at a high logic state, if the first comparison information is at the high logic state, or

at a low logic state, if the second comparison information is at the high logic state, or

at its previous logic state, if one of the first comparison information and the second comparison information is at the low logic state.

21. (original) A channel state measurement apparatus for a receiver that provides channel state information in accordance with the method of claim 10.

22. (original) An apparatus for providing channel state information in a receiver in accordance with the method of claim 10.